VERSION SHOWING AMENDMENTS TO THE CLAIMS

This listing replaces all prior listings of the claims.

IN THE CLAIMS

Amend the claims as follows:

1 (Currently amended). An organic field effect transistor (OFET) including a gate, comprising:

a first electrode layer forming source and drain electrodes each having multiple sides ;

a semiconducting layer;

an insulator layer;

one of the source and drain electrodes in the first electrode layer surrounding the respective other electrode of the first electrode layer in a two-dimensional manner with the exception of one of said sides of the other electrode; and

a second electrode layer forming a gate electrode, the semiconducting layer exhibiting a current channel in the presence of an applied voltage and wherein the second electrode layer completely overlies the current channel and overlies a portion of the source or drain electrodes of the first electrode layer, the overlying portion with respect to the source or drain electrodes having a width solely in the range from about 0 to about 20 μm and having a length in the range of the length of the current channel to thereby minimize parasitic capacitance that otherwise might occur;

whereby a u-shaped and/or meandering current channel , which begins and ends on one of said sides of the electrode of the first electrode layer is formed in the semiconducting layer.

2 (Previously presented). The OFET as claimed in claim 1 wherein the first electrode layer respectively bounds the other electrode layer on three of four sides.

Claim 3, canceled.

4 (Previously presented). The OFET as claimed in claim 1 wherein holes and/or interruptions are in the semiconductor layer to reduce leakage currents.

5 (Previously presented). An integrated circuit having at least two OFETs as claimed in claim 1 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

6 (Previously presented). The integrated circuit as claimed in claim 5 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

7 (Previously presented). The integrated circuit as claimed in claim 5 wherein holes and/or interruptions are in the semiconductor layer.

8 (Previously presented). The integrated circuit as claimed in claim 7 wherein the holes and/or interruptions are between the one sides .

9 (Previously presented).The integrated circuit as claimed in claim 5 including a through-contact in said first electrode layer.

10 (Previously presented). The integrated circuit as claimed in claim 9 wherein the through-contact extends at least to one further side of the OFET other than said one side.

Claim 11, canceled

12 (Previously presented). The OFET as claimed in claim 2 wherein holes and/or interruptions are in the semiconductor layer to reduce leakage currents.

13 (Previously presented). The OFET as claimed in claim 3 wherein holes and/or interruptions are in the semiconductor layer to reduce leakage currents.

14 (Previously presented). An integrated circuit having at least two OFETs as claimed in claim 2 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

15 (Previously presented). An integrated circuit having at least two OFETs as claimed in claim 3 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

16 (Previously presented). An integrated circuit having at least two OFETs as claimed in claim 4 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

17 (Previously presented). The integrated circuit as claimed in claim 14 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

18 (Previously presented). The integrated circuit as claimed in claim 15 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

19 (Previously presented). The integrated circuit as claimed in claim 16 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

Claim 20, canceled